## REMARKS

This amendment is in response to the Final Office Action dated November 29, 2006. Claims 1-19 are pending. The current status of the claims is summarized below. Support for the amendment exists throughout the specification and hence no new matter has been entered. Applicants respectfully request reconsideration of the application in view of the following remarks submitted in support thereof.

**Rejections under 35 U.S.C. § 103:**

Claims 1-19 were rejected under 35 U.S.C. § 103(a), as being unpatentable over Shimogori (U.S. Patent Application No. 2002/0152061A1) (hereinafter Shimogori) in view of Shridhar et al. (U.S. Patent No. 5,815,714) (hereinafter Shridhar). This rejection is respectfully traversed.

With reference to independent claims 1, 6, 9 and 15, the primary reference of Shimogori does not suggest or teach each and every element of the currently amended independent claims 1, 6, 9 and 15. The Examiner equates "identifying a block level location having an error from a first simulation" of the instant application with identifying what parts of C language source code can be speeded up through conversion to VU (conversion to hardware) instructions. The Applicants defer from the Examiner's assertion of equating parts of C language code to the block level having an error of the instant application.

The Examiner further asserts that Shimogori teaches "inserting a patch into ***a thread specific to the block level location of the error***". Shimogori teaches identifying a portion of a code that can be speeded up by converting relevant software code to hardware instructions. The identified piece of software code is extracted from the executing function and replaced with a hardware (VU) instruction (patch). By replacing the identified piece of code, the

patch takes care of what the Examiner constitutes as an "error". Therefore, there is no need to further "execute a second simulation to determine **a signal level location** of the error through information generated by the patch" or to "correct the code representation of a processor associated with the error" since what the Examiner refers to as an error (the extra clock cycles) have been addressed by the hardware patch. Consequently, the patch of Shimogori can not generate any information regarding the signal level location of the error as the error has already been addressed.

The Examiner's portrayal of an "error" in Shimogori is not actually an error. The number of clock cycles that a particular piece of code takes, in Shimogori, does not constitute an error that may cause drastic consequences if left undetected. The "error" in Shimogori is more a performance delay that is overcome by the "patch". The error, in the claimed invention, is a defect in a chip that when undetected can cause drastic consequences during the manufacturing phase of the chip. Further, in the claimed invention, a patch is inserted at an identified block level location based on output data from a first simulation. The output data of the claimed invention identifies an error and the location of the error (at a block level) which is significantly different from Shimogori's clock cycle comparison which does not identify an error or the location of the error. Moreover, Shimogori does not have to run a second simulation to see if the patch addresses the "error".

In contrast, the instant application deals with simulation of complex processor architecture by identifying **block level location of the error** within the processor circuit during a first simulation, inserting a patch at the identified block level location of the error to further identify a **signal level location** of the error within the identified block, executing a second simulation to determine the signal level location of the error through information generated by the patch and correcting a code representation of a processor circuit associated with the block having the error. By identifying the errors first at the block level and then at

the signal level, the errors can be identified faster and corrected more efficiently instead of sifting through a number of error signals and manually determining which block is at issue. (See page 14, lines 4-8, page 16, lines 24 through page 17, line 2).

Applicants, therefore, submit that the reference of Shimogori does not suggest or teach each and every element of the claimed invention and request the Examiner to withdraw the rejection on the independent claims 1, 6, 9 and 15. Claims 2-4, 7, 8, 10-14 and 16-18 depend from independent claims 1, 6, 9 and 15 respectively. Shridhar does not cure any of the above mentioned deficiencies of Shimogori. Based on the arguments presented, Applicants request that the 103 rejections be withdrawn and claims 1-4, 6-9, 11-18 be allowed.

A Notice of Allowance is respectfully requested. If the Examiner has any questions concerning the present Amendment, the Examiner is kindly requested to contact the undersigned at (408) 774-6905. If any other fees are due in connection with filing this Amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. ADAPP222). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
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